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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,865	01/15/2004	Minoru Fujishima	44471/296251	8418

23370 7590 04/19/2005

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EXAMINER	
NGUYEN, MINH T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/759,865	FUJISHIMA, MINORU	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *11-16 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 17-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/2/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's response filed on 3/23/05 to the restriction/election requirements without traverse is acknowledged. The restricted claims can be rejoined later if the generic claims are found allowable. The following is a detailed office action of the elected claims, i.e., claims 1-10 and 17-19.

Claim Objections

2. Claim 6 is objected to because of the following informalities: line 2, "third ½ divider" should be changed to -- third ½ dividers -- to avoid potential antecedent basis problem, see line 3 of claim 5.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The recitation "a switch signal stopping operation of the third divider" is misdescriptive because as disclosed in the specification, the switch is merely for stopping the supply of the third high frequency signal to the mixer, not for stopping the operation

of the third divider. In other words, the switch does not stop the operation of the third divider as recited.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-10 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 4,855,895, issued to Shigaki et al. in view of US Patent No. 4,633,194, issued to Kikuchi et al.

As per claim 1, Shigaki discloses a frequency divider (figure 5) comprising:

a first divider (the divider 4) configured to divide an input signal (INPUT SIGNAL), and to generate a first high frequency signal (the signal having the frequency F/P at the output of the divider 4);

a third divider (the divider 2) configured to generate a third high-frequency signal (the signal having the frequency X/N at the output of the divider 2); and

a mixer (MIXER 1) configured to execute arithmetic processing for the first and third high-frequency signals, and to generate the second high-frequency signal (the signal having the frequency X).

Shigaki further explicitly discloses the second high frequency signal is the output signal of the frequency divider circuit. Therefore, in general, the Shigaki's frequency divider circuit can be seen as further including a second divider circuit having a division

ratio of one for dividing the second high frequency signal (X) and generate the output signal (DIVIDED SIGNAL) having the same frequency as the second high frequency signal.

Shigaki does not explicitly disclose a second divider which divides the second high frequency signal to generate an output signal as called for in the claim.

Kikuchi discloses a frequency divider (figure 1) including a second divider (12) for dividing the second high frequency signal to generate an output signal (3).

It would have been obvious to one skilled in the art at the time of the invention was made to include a second divider between the mixer MIXER1 and the third divider in the Shigaki's frequency divider circuit. The motivation would be to provide more control of the frequency of the output signal.

As per claim 2, the combination which is discussed in claim 1 clearly includes the recited structure.

As per claims 3-4, as shown in figure 5 of the Shigaki's reference, the feedback configuration of the third divider clearly indicates the subtraction processing in the mixer circuit.

As per claim 5, Shigaki discloses a generic frequency divider (figure 1) which comprises a plurality of stages of cascaded connected 1/2 dividers (also see column 1, lines 36-45).

As per claim 6, as shown in figure 4, switch 3 can be optionally included in the frequency divider circuit to stop outputting the third frequency signal to the mixer.

As per claim 7, the combination which is discussed in claim 1 clearly discloses the division ratios of the dividers are variable.

As per claim 8, the combination discussed in claim 2 does not disclose the recited limitation that a filter is included in between the third divider and a mixer as called for in the claim.

However, as known by a person skilled in the art, noisy signal is not desirable because "garbage in would produce garbage out" in an electronic circuit, and it's also known that noisy signal can be clean by passing the signal through a filter.

It would have been obvious to one skilled in the art at the time of the invention was made to include a filter between the third divider and the mixer in the combination discussed in claim 2. The motivation would be to provide a clean third frequency signal to the mixer so that accurate signal can be output at the output of the mixer.

As per claim 9, this claim is rejected for the same reason noted in claim 6.

As per claim 10, the combination discussed in claim 2 does not disclose a switch circuit is included in between the second divider and third divider as called for in the claim.

However, it is clear that placing the switch circuit between the second divider and the third divider or between the third divider and the mixer serves the same purpose which is to allow the control of the act of providing or stopping the supply of the third clock signal to the mixer. Placing the switch circuit in either location is merely a rearranging of the parts in the frequency divider circuit. It has been held by the court that rearranging of the elements in a circuit is not patentable. It's further known that changing locations of elements in a circuit can increase or decrease the electromagnetic interference caused by the high frequency of the signals in the circuit.

It would have been obvious to one skilled in the art at the time of the invention was made to rearrange the switch circuit in the Shigaki's frequency divider between the second divider and the third divider instead of between the third divider and the mixer. The motivation would be to minimize the electromagnetic interference caused by the high frequency of the signals in the Shigaki's frequency divider.

As per claim 17, this claim is rejected for the same reason noted in claim 1. The recited semiconductor integrated circuit taught in column 5, lines 13-15.

5. Claims 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 4,633,194, issued to Kikuchi et al. in view of US Patent No. 4,855,895, issued to Shigaki et al

As per claim 18, Kikuchi discloses a phase locked loop circuit (figure 4) comprising:

a comparison oscillator (VCO 34) configured to generate an oscillation signal (the signal having the frequency F0) having a frequency corresponding to a phrase difference between a reference clock and a comparison clock (this is a standard function of any phase locked loop circuit); and

a frequency divider (30) configured to divide the oscillation signal wherein the frequency divider (30) is adjustable.

Kikuchi does not explicitly disclose the frequency divider configured to generate a first high-frequency signal, and to divide a second high-frequency signal, and to generate a third high-frequency signal, and to execute arithmetic processing for the first

and third high-frequency signals and to generate the second high-frequency signal as called for in the claim.

Shigaki discloses a frequency divider (figure 4) which performs the recited function as discussed in claim 1.

It would have been obvious to one skilled in the art at the time of the invention was made to replace the Kikuchi's frequency divider 30 by the frequency divider discussed in claim 1 herein above. The motivation would be to allow the Kikuchi's PLL to operate in applications which are operated with high frequency signals since Shigaki's frequency divider can be very efficient when working with high frequency signals as explicitly disclosed in the Shigaki's reference (see the summary of invention section).

As per claim 19, the structure of Shigaki's frequency divider meets the recited limitation as discussed in claim 1.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is **571-272-1748**. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

4/15/05

Minh Nguyen
Primary Examiner
Art Unit 2816